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View a complete reference design of this system simulation and rapid prototyping and see a demonstration of a real-time simulation of a 3-phase single-level inverter with RLC filter and load. The real-time HIL simulation is executed in FPGA hardware using LabVIEW at a 1 MHz loop rate.

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Simulation typically steps through the operation of the testbench, which stimulates the FPGA. The simulation process observes the transformations and translations of signals as they propagate through the FPGA from the input pins and provides responses that eventually reach an output pin.

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